

Modelling the generic TiO_2 memristor with the parasitic components

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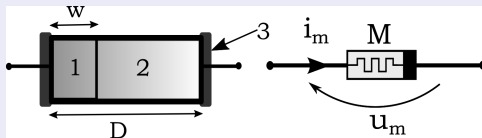
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Problem description

Memristor is the famous fourth basic electric circuit element postulated by Leon Chua in 1971. The discovery of the physical solid-state structures having memristive characteristics by the HP scientists in 2008 has attracted enormous interest in the scientific community.



Model of the memristor and its equivalent symbol. (1-doped region (TiO_{2-x}), 2-undoped region (TiO_2), 3-metal contact)

The HP memristor is a nano-scale sandwich-like structure build on the TiO_2 and oxygen-poor TiO_{2-x} between two platinum electrodes. The total thickness of this structure is denoted by the parameter D . If one applies some voltage across this structure the electric field the TiO_{2-x} layer changes its thickness w with the average mobility of the oxygen vacancies μ_v . So the functions of $w(t) \in (0, D)$ depend on the electrical variables that the memristor is subject to. The relations between the voltage and current can be formulated as:

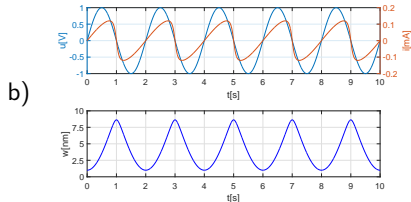
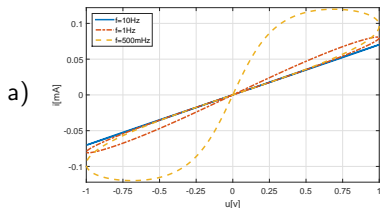
$$u_m(t) = \left[\mathcal{R}_{ON} \frac{w(t)}{D} + \mathcal{R}_{OFF} \left(1 - \frac{w(t)}{D} \right) \right] i_m(t) \quad (1)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{\mathcal{R}_{ON}}{D} i_m(t) \quad (2)$$

The \mathcal{R}_{ON} and \mathcal{R}_{OFF} are the minimum and maximum resistance for $w = D$ and $w = 0$, respectively.

Memristor sinusoidal response

- a) - The typical zero-crossing pinched hysteresis loop as the memristor response for the sinusoidal excitation ($U_{\max} = 1V$).
- b) - The voltage and the current in the memristor and the $w(t)$ function vs time t for $f = 0.5Hz$.

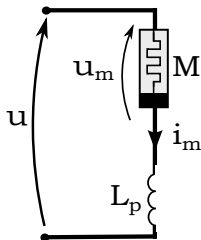


The presented graphs has been achieved using the typical HP memristor parameters:

$$\mathcal{R}_{ON} = 100 \Omega, \mathcal{R}_{OFF}/\mathcal{R}_{ON} = 160, \mu_v = 10^{-10} \text{ cm}^2\text{s}^{-1}\text{V}^{-1}, D = 10 \text{ nm}, U_{max} = 1 \text{ V}.$$

In reality the memristors have some parasitic parameters which should be taken into consideration. As memristor has the sandwich like structure it has some parasitic capacitance. Also parasitic inductance should be considered as the solid-state structure is connected to the environment by wires.

Memristor with parasitic inductor



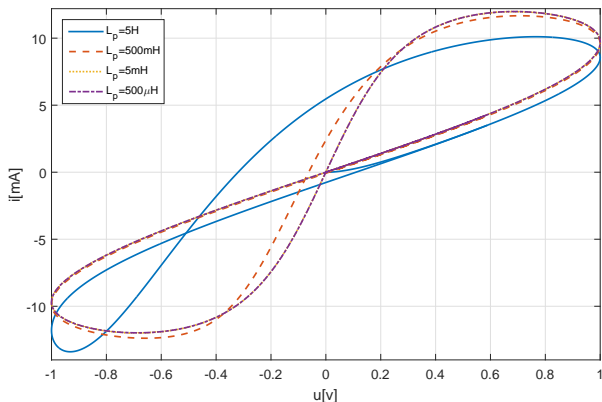
Parasitic inductor L_p connected in series with the memristor M

Two dimension state equation is as follow:

$$\begin{cases} \frac{di_m}{dt} = \frac{1}{L_p} (u(t) - (\mathcal{R}_{ON}z(t) + \mathcal{R}_{OFF}(1 - z(t))) i_m(t)) \\ \frac{dz}{dt} = \mu_v \frac{\mathcal{R}_{ON}}{D^2} i_m(t) \end{cases} \quad (3)$$

Where $z(t) = w(t)/D \in [0, 1]$.

Memristor with parasitic inductor



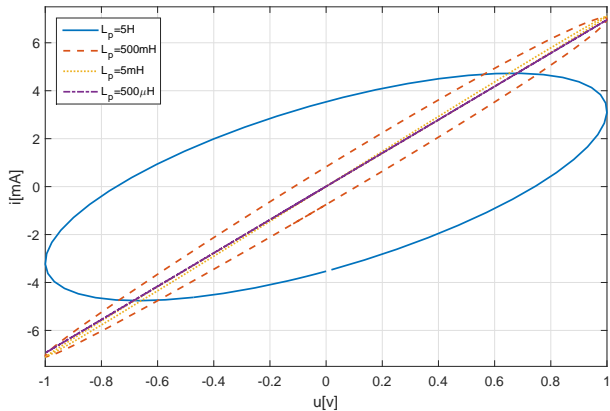
The pinched hysteresis loop of the memristor with the presence of parasitic inductance L_P ($f = 0.5\text{Hz}$).

Memristor with parasitic inductor

The coordinates of the pinched points for different parasitic inductance values ($f = 0.5\text{Hz}$).

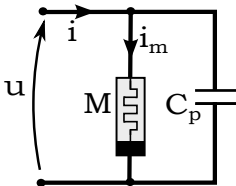
L_p	U [mV]	I [μA]
5H	-509.7	-4545.5
500mH	-78.23	-619.3
50mH	-8.575	-72.7
5mH	-0.831	-5.765
500 μH	-0.0697	-1.266

Memristor with parasitic inductor



The v - i characteristics for different parasitic inductive component for the frequency $f = 5\text{Hz}$.

Memristor with parasitic capacitor

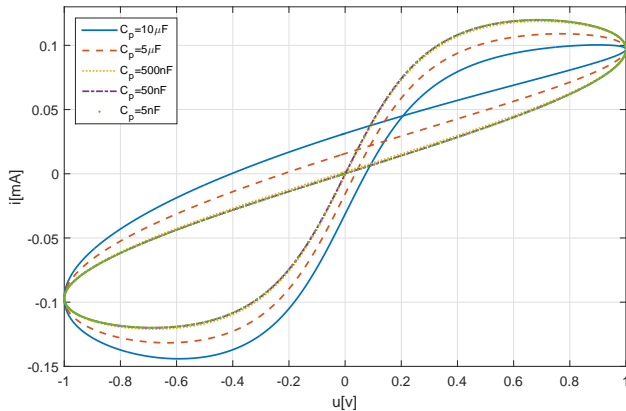


Parasitic capacitor C_p connected in parallel with the memristor M

The basic equation is:

$$i = i_m + C_p \frac{du}{dt} \quad (4)$$

Memristor with parasitic capacitor



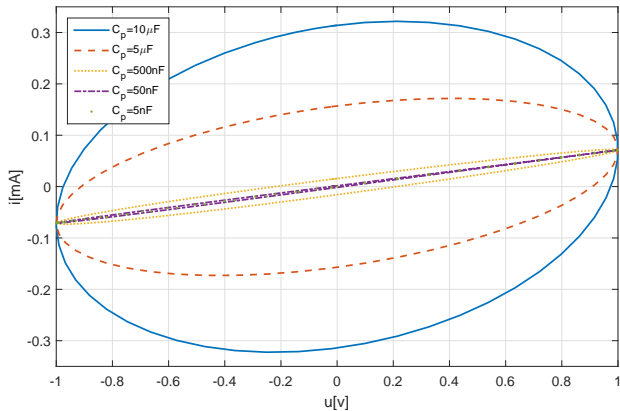
Pinched hysteresis loop of the memristor with different parasitic capacitance component for the frequency $f = 0.5\text{Hz}$.

Memristor with parasitic capacitor

The coordinates of the pinched points for different parasitic capacitance values ($f = 0.5\text{Hz}$).

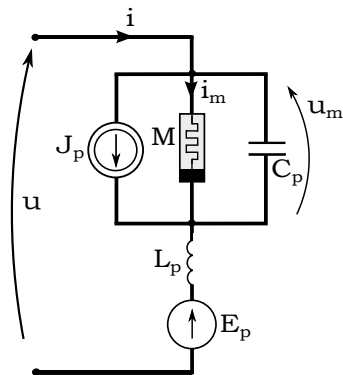
C_p	U [mV]	I [μA]
$10\mu\text{F}$	206	45.1
$5\mu\text{F}$	88.7	21.8
500nF	8.52	2.163
50nF	0.862	0.2162
5nF	0.086	0.217

Memristor with parasitic capacitor



The v - i characteristics for different parasitic capacitance component for the frequency $f = 5\text{Hz}$.

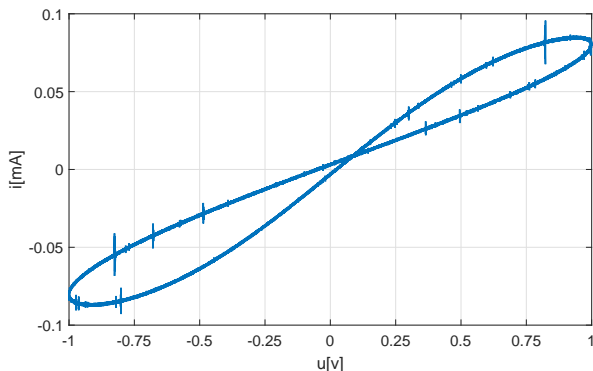
Memristor model with the parasitic elements



State equations for the memristor model with parasitic components.

$$\begin{cases} \frac{du_m}{dt} = \frac{1}{C_p} (i - J_p - i_m) \\ \frac{di}{dt} = \frac{1}{L_p} (u - u_m - E_p) \\ \frac{dz}{dt} = \mu_v \frac{\mathcal{R}_{ON}}{D^2} i_m(t) \end{cases} \quad (5)$$

Memristor model with the parasitic elements



The pinched hysteresis loop of the memristor model with parasitic components $L_p = 5$ mH and $C_p = 1$ μ F for $f = 0.5$ Hz. The pinched point is shifted to $(u, i) \rightarrow (41.1\text{mV}, 7.16\mu\text{A})$.

Memristor model with the parasitic elements

Change the voltage source with the current source

$$u(t) \rightarrow j(t) = J_{\max} \sin(2\pi ft)A$$

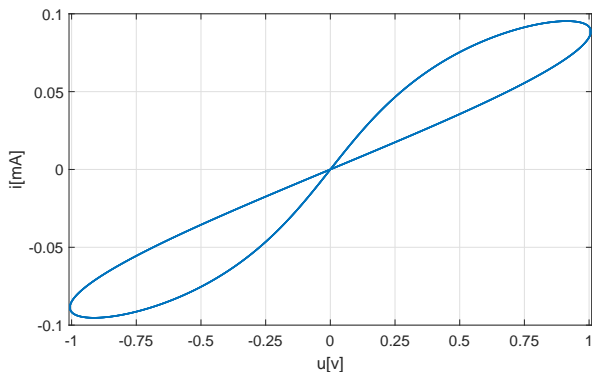
Then the state equation is reduced to 2nd dimension:

$$\begin{cases} \frac{du_m}{dt} = \frac{1}{C_p} (j - i_m) \\ \frac{dz}{dt} = \mu_v \frac{R_{ON}}{D^2} i_m(t) \end{cases} \quad (6)$$

This approach makes the calculations much faster and more stable.

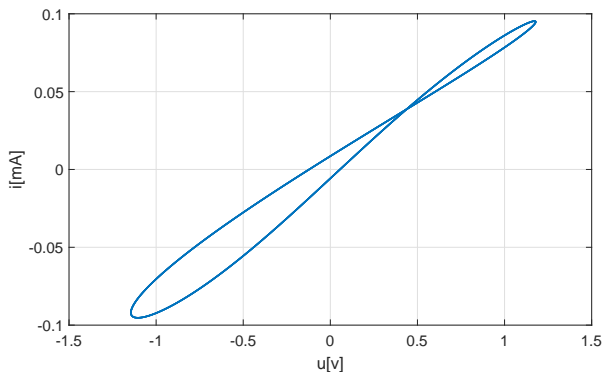
If the maximum value of the current source is $J_{\max} \approx 95.3\mu A$, the voltage response belongs to the interval of $[-1, 1]$ volts and the graph is nearly the same as on the previous graph.

Memristor model with the parasitic elements



The hysteresis loop of the memristor model with parasitic components $L_p = 5 \mu\text{H}$ and $C_p = 5 \text{nF}$ for $f = 0.5 \text{ Hz}$.
The pinched point is shifted to $(u, i) \rightarrow (210 \mu\text{V}, 37 \text{nA})$.

Memristor model with the parasitic elements

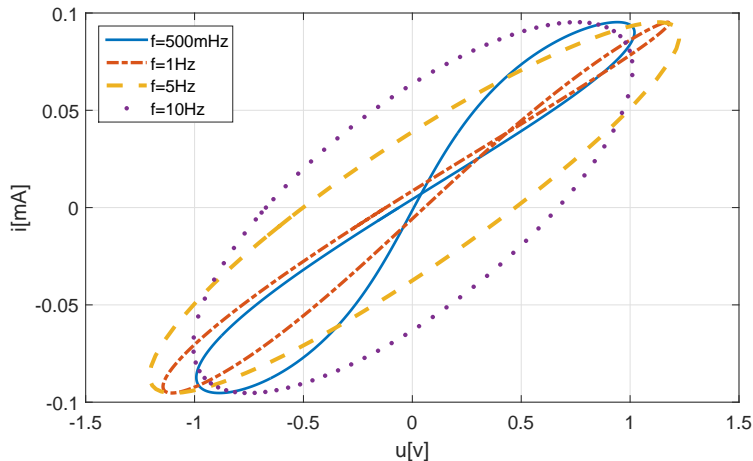


Hysteresis loop of the memristor model with parasitic components

$$L_p = 5 \text{ mH} \text{ and } C_p = 1 \mu\text{F} \text{ for } f = 1 \text{ Hz.}$$

The pinched point is shifted to $(u, i) \rightarrow (436\text{mV}, 38.5\mu\text{A})$.

Memristor model with the parasitic elements



The hysteresis loop of the memristor model with parasitic components $L_p = 5 \text{ mH}$ and $C_p = 1 \mu\text{F}$ for variable frequencies.

The tested inductance and capacitance values are much higher than those that we can meet in reality. The experimental results show that the capacitance and inductance can reach the values of some nano Farads and some tens of nano Henrys accordingly.

When the single memristor works at the low frequency its parasitic components may be neglected, but in many applications, for example, when the memristor arrays are used the problem returns and deeper studies are necessary.

References:

- [1] L.O. Chua, *Memristor-the missing circuit element*, IEEE Trans. Circuit Theory, vol. CT-18, no. 5, pp. 507-519, 1971
- [2] D.B. Strukov, G.S. Snider, D.R. Steward and R.S. Williams, *The missing memristor found*, Nature, vol. 435, pp. 80-83, 2008
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- [4] A. Kumar and M.S. Baghini, *Experimental study for selection of electrode material for ZnO-based memristors*, ELECTRONICS LETTERS, vol.50(21), pp.1547-1548, 2014