Investigations of switching phenomena in $Pt/HfO_2/Ti/Pt$ memristive devices

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Problem description

Abstract

- In the presentation, the results of time-domain laboratory measurements of memristive devices are going to be shown.
- Authors studied the dynamics of the process of memristor forming and investigated switching mechanisms in memristors.
- Measurement results are compared with a standard model of oxide-based memristor.
- It is going to be confirmed that endurance may be a problem for this type of memristors.

Problem description

In real applications, the most interesting questions are:

- What are the switching characteristics of memristors?
- What are the transition characteristics between the stable resistance states in multi-level memristive elements?
- How big are the charges/energies to cause the switch between the stable states?
- How fast the memristive switches can operate?
- What are the best characteristics for write-in and read-out?

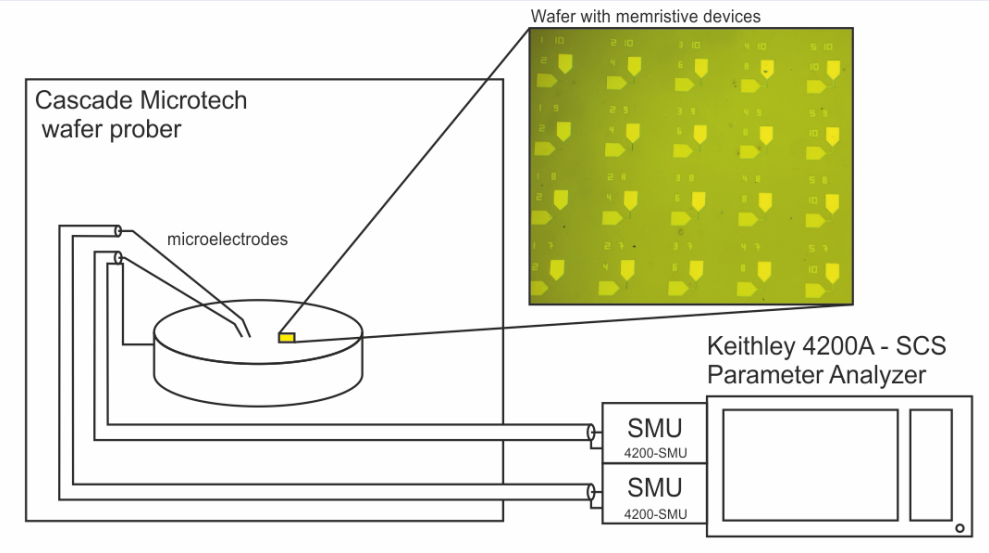
Measurement Results

The physical construction of the memristor device

- The tested device was a Metal-Insulator-Metal (MIM) structure, with a stack of the Pt/HfO_2/Ti/Pt structure.
- Each device consists of two crossing lines of Pt with a width ranging from $2\,\mu$m to $10\,\mu$m and 10 nm-thick Ti layer.
- All the tested elements were fabricated in the LSI lab (Integrated Systems Laboratory) at EPF (ECOLE POLYTECHNIQUE FEDERALE) in Lausanne.

Measurements

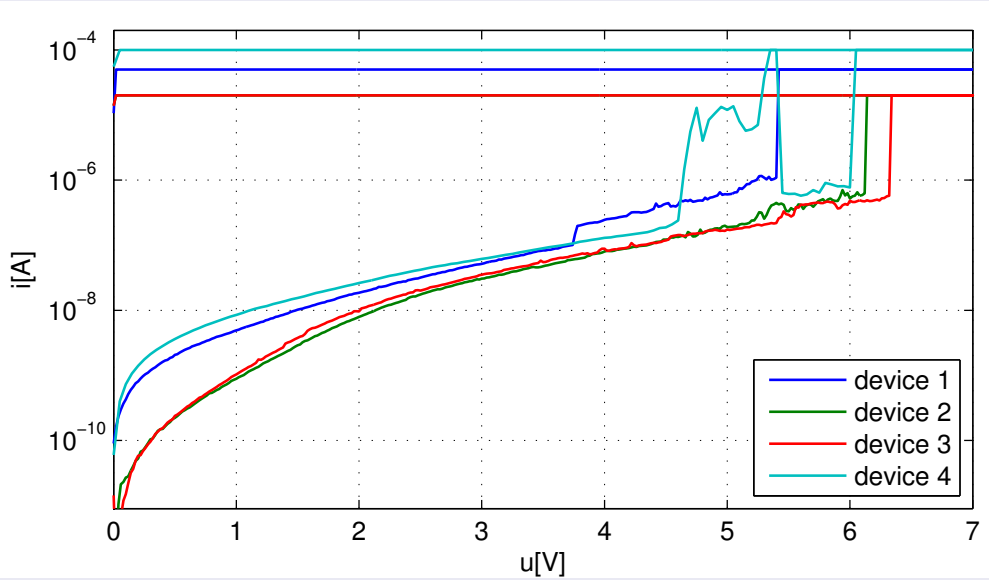
Experimental set up



Simplified diagram of the experimental set-up. The wafer with test structures was placed on a vacuum chuck of the Cascade Microtech wafer prober. Two micromanipulators with passive tungsten needles were attached to the pads of the devices under test (DUT). Probes were connected to the two source-measure units (SMUs) of the Keithley Model 4200SCS Semiconductor Parameter Analyser using SMA coaxial cables.

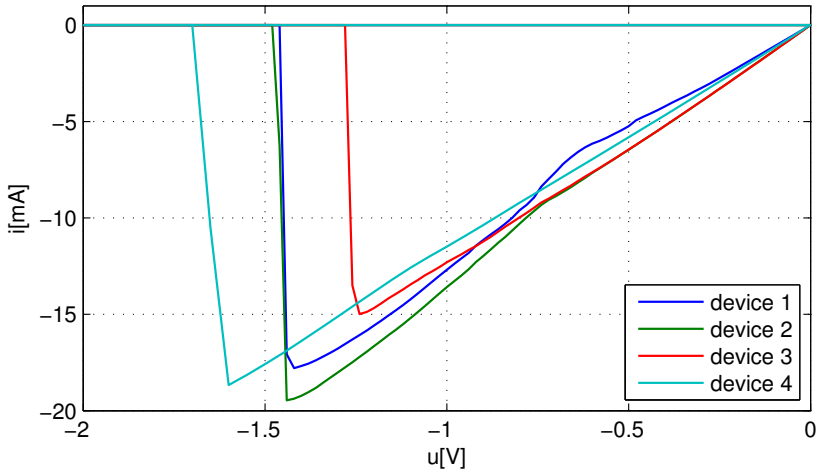
Measurements

Forming

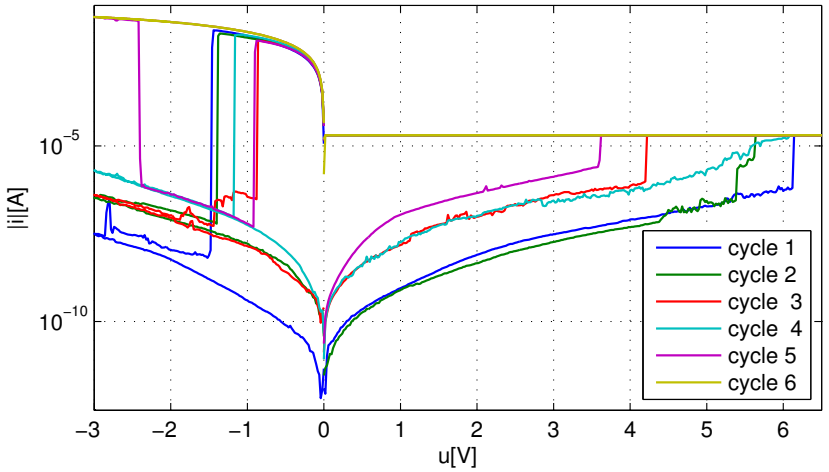


The forming process of 4 different memristor devices. For the first three devices, the voltage sweep rate is $\mathrm{dV/dt} = 0.25\,\mathrm{V}\cdot\mathrm{s}^{-1}$, while for the last one it is $\mathrm{dV/dt} = 0.5\,\mathrm{V}\cdot\mathrm{s}^{-1}$. The protecting current limit was set to be $I_\mathrm{C} = 20\,\mu\mathrm{A}$ for the first two devices, $I_\mathrm{C} = 50\,\mu\mathrm{A}$ for the third device, and $I_\mathrm{C} = 100\,\mu\mathrm{A}$ for the fourth device.

Setting and resetting cycles

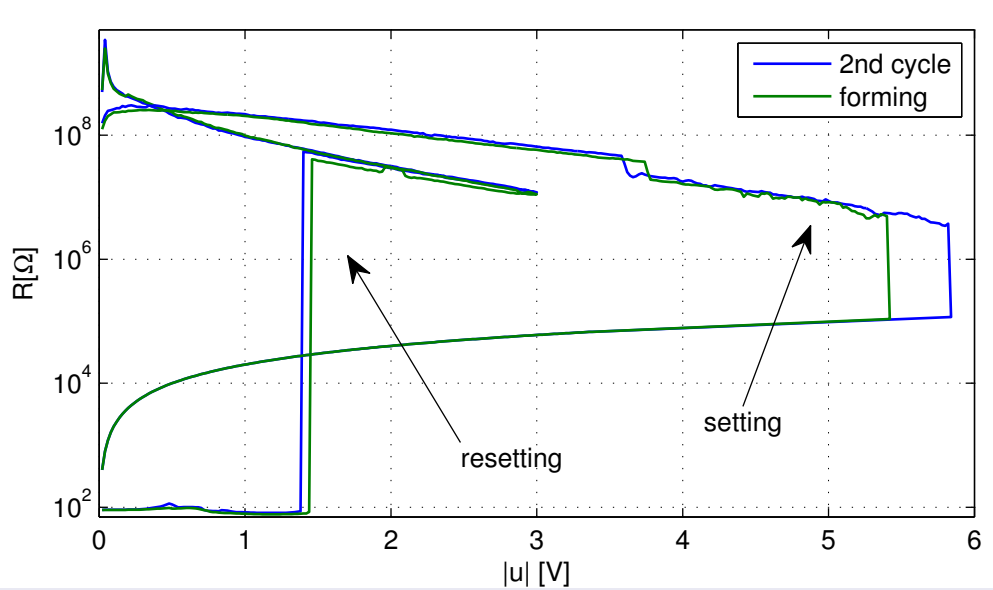


Switching the elements from the ON state to the OFF state



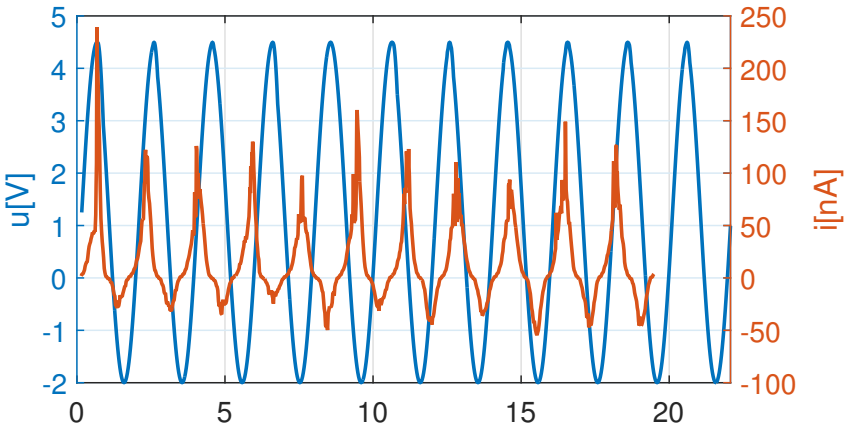
The six cycles of switching to the ON state and to the OFF state for the third DUT. The absolute value of the current is plotted in the logarithmic scale.

Resistance profiles during switching

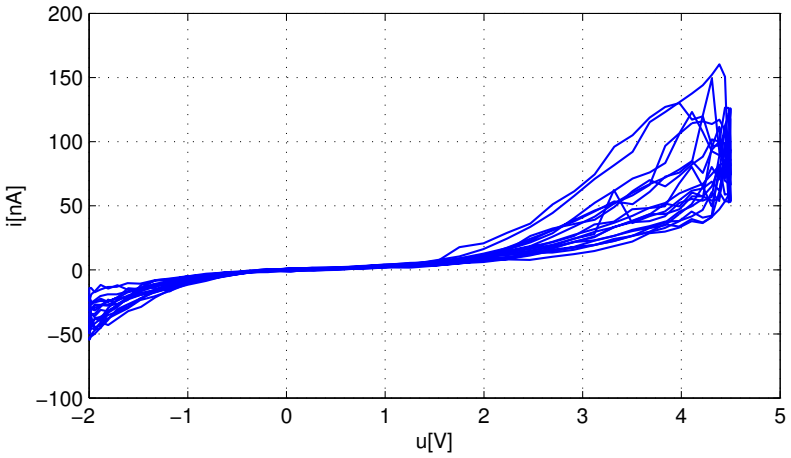


The plot of the resistance changes for the setting and resetting processes versus the absolute value of the voltage for an example DUT.

Sinusoidal excitation



Plot of the voltage and current vs time. $u = \{3.25 \sin(2\pi \cdot 0.538\ t) + 1.25\}\ [\mathrm{V}]$



Voltage-current plot

Fitting measurements to a memristor model

For modelling it has been selected the physics-based model of tantalum oxide memristors introduced by: J. P. Strachan, A. C. Torrezan, F. Miao, M. D. Pickett, W. Y. J. J. Yang, G. Medeiros-Ribeiro, and R. S. Williams, in "State dynamics and modeling of tantalum oxide memristors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2194–2202, 2013.
In this model, the dynamics of the memristor is given by:

$$\frac{\mathrm{d}x}{\mathrm{d}t} = g(x, v_m), \quad i_m = G(x, v_m)v_m, \tag{1}$$

where i_m and v_m denote the current and the voltage of the memristor. Equations (1) define a voltage-controlled memristor. The internal variable $x \in [0, 1]$ represents the volume fraction with metallic transport. $G(x, v_m) = G_m x + a \exp\left(b\sqrt{|v_m|}\right)(1 - x)$ is the conductance of the device.

Fitting measurements to a memristor model

$$\frac{\mathrm{d}x}{\mathrm{d}t} = g(x, v_m), \quad i_m = G(x, v_m) v_m,$$

The function $g(x, v_m)$ defining the dynamics of the internal state $x \in [0, 1]$ is zero if $x = 0$ and $v_m \leqslant 0$ or if $x = 1$ and $v_m \geqslant 0$. Otherwise

$$g(x, v_m) = A \sinh\left(\frac{v_m}{\sigma_{\mathrm{off}}}\right) \exp\left(-\frac{x_{\mathrm{off}}^2}{x^2}\right) \exp \frac{1}{1 + \beta_m p_m}$$

for $v_m < 0$ and

$$g(x, v_m) = B \sinh\left(\frac{v_m}{\sigma_{\mathrm{on}}}\right) \exp\left(-\frac{x^2}{x_{\mathrm{on}}^2}\right) \exp \frac{p_m}{\sigma_p}$$

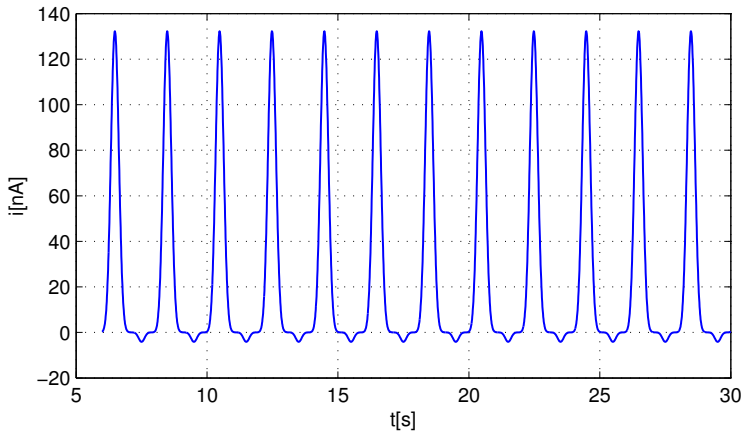
for $v_m \geqslant 0$, where $p_m = v_m i_m = G(x, v_m) v_m^2$.

Fitting measurements to a memristor model

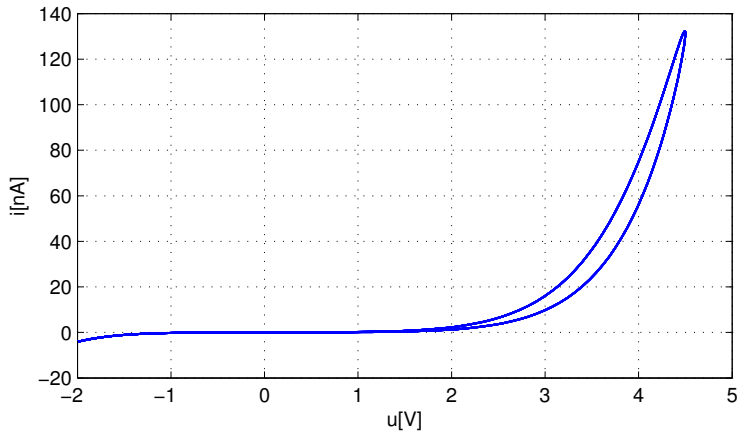
- Matching the model presented before was to the data observed for the sinusoidal input.
- In the matching procedure to remove the noise, an average current waveform with the length equal to the period of the input signal has been computed.
- The optimization goal was to minimize the mean square error between the averaged measured current for the sinusoidal input and the steady state periodic current obtained in simulations for the same input.
- The best match has been observed for the following parameters: $a = 10^{-12}\,\mathrm{S}$, $Gm = 10^{-10}\,\mathrm{S}$, $b = 5.5\,\mathrm{V}^{-1}$, $A = 10$, $\sigma_{\mathrm{off}} = 0.01\,\mathrm{V}$, $x_{\mathrm{off}} = 0.7$ $\beta_m = 300\,\mathrm{W}^{-1}$, $B = 90$, $\sigma_{\mathrm{on}} = 0.6\,\mathrm{V}$, $x_{\mathrm{on}} = 0.2$, $\sigma_p = 5 \times 10^{-7}\,\mathrm{W}$.

Fitting measurements to a memristor model

A steady-state results of applying the waveform $u(t) = (1.25 + 3.25\sin(2\pi f t))\,\mathrm{V}$, with the frequency $f = 0.538\,\mathrm{Hz}$



Plot of the voltage and current vs time.



Voltage-current plot

- authors were able to roughly match the amplitudes of the current and that the hysteresis loop is well visible in simulations
- precise matching is not possible due to the noisy input data.

Discussion of results

- The results of laboratory measurements of $Pt/HfO_2/Ti/Pt$ memristive devices has been carried out.
- It has been shown that memristors fabricated in this technology display high variability in dynamical behaviors and in particular the lack of repeatability of measurements from cycle to cycle.
- The experiments confirm a low endurance of the tantalum oxide-based elements which has also been observed by other researchers.

Discussion of results

- In all tests, the memristors suffered from the so-called wear-out problem—after many ON-OFF cycles.
- The wear-out phenomenon is recognized also in practical circuit realizations—a solution for avoiding worn-out elements in memristive memory arrays has been patented [1].
- Results from the I. Valov group [2] suggest that there is a lack of symmetry in the ON and OFF processes, i.e. not exactly the same number of atoms undergo recombination when the voltage swing changes sign thus after a larger number of switchings the elements loose their properties—wear-out.
- The existing physics-based model has been fitted to match the measurement data for the sinusoidal forcing case. The best match we were able to find is far from being perfect and further investigations have to be carried out.

[1] Y. Kang, "Method and apparatus managing worn cells in resistive memories," US Patent 8634225 B2, Samsung Electronics Co. Ltd., 2014.

[2] A. Wedig, M. Luebben, D.-Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepali, B. Yildiz, R. Waser, and I. Valov, "Nanoscale cation motion in taox, hfox and tiox memristive systems," *Nature Nanotechnology*, vol. 11, pp. 67–74, 2016.

Thank You
For Your Attention