A Data-Driven Noise Modelling Paradigm for Analog TiO_2 Devices

Ioannis Messaris[1]*, Alexander Serb[2], Themis Prodromakis[2] and Maciej Ogorzalek[3]

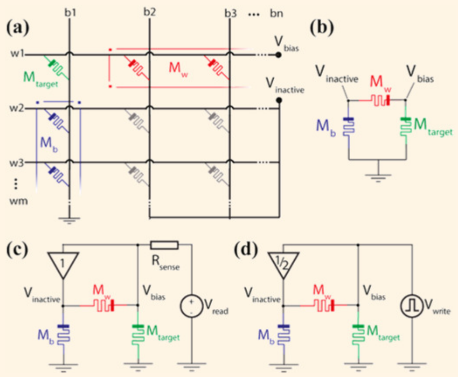
[1]*Faculty of Electrical and Computer Engineering, TU Dresden, Dresden, Germany*
[2]*Nano Group, ECS, University of Southampton, Southampton, England*
[3]*Department of Information Technologies, Jagiellonian University Krakow, Krakow, Poland*
**Corresponding author e-mail: ioannis.messaris@tu-dresden.de*

Introduction:

In this work we quantify noise in experimental resistive responses of analog $TiOx$-based samples provoked by pulse trains of constant bias voltage amplitude which is a biasing scheme that has been widely adopted for modulating memristor resistance. Device stochastic switching behavior aggregated with instrument induced noise is captured for resistive responses provoked by various voltage levels and subsequently integrated in a recently presented ReRAM model [1]. The method used is rather uncomplicated and can be easily plugged in current characterization tools [2].

Motivation:

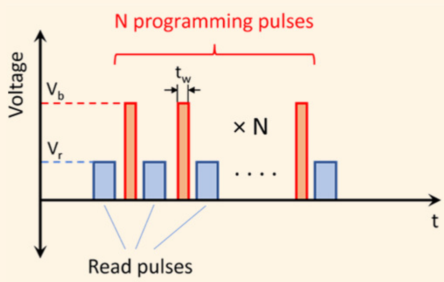
The programmable resistor property in memristors offers great potential for implementing reconfigurable basic analog circuits such as filters, gain amplifiers, comparators etc. ([3], [4]). Nevertheless, implementing suitable circuit components for tuning accurately memristor resistance requires considering non-ideal effects such as noise in the simulation stage of the overall design flow.



- $N \times N$ crossbar array. (c) and (d) demonstrate conceptual circuits for performing reading and writing operations on an arbitrary ReRAM device.
- Device resistance must be assessed multiple times in the tuning process.
- The corresponding circuit elements (for example Transimpedance Amplifiers depicted with 1 and ½ in figure) also contribute noise and thus measurement uncertainty.

Device Characterization:

- Switching noise in the device operating resistive region $[R_{min}, R_{max}]$ is characterized for multiple voltage levels V_b of both polarities.
- For each voltage level V_b we apply a pulse train of N identical pulses of fixed pulse duration t_w.



- Initial device resistance R_0 and the resistance after each single pulse applied $R_0 + \Delta R$ are measured.
- All assessments of resistance state are carried out at the standard read voltage $V_r = 0.2\,V$.
- Characterization protocol parameters: $N = 500\,pulses/train$, $t_w = 100\mu s$pulse trains with the following amplitudes are applied in sequence:

$$V_b = \{-1.2\,V, 1.7\,V, -1.3\,V, 1.8\,V, -1.4\,V, 1.9\,V, -1.5\,V\,, 2.0\,V\}$$

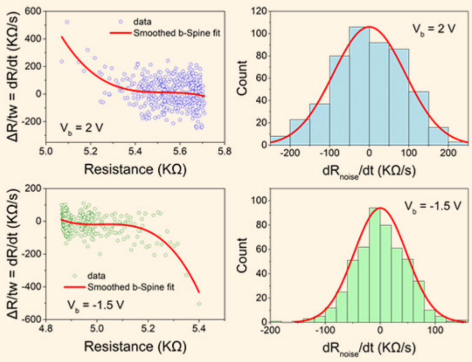
Data Processing

- As a first approximation we assume that switching noise depends solely on voltage (and not device resistance): $N_{sw}(v)$
- Switching noise N_{sw} is captured by plotting amount of switching ΔR versus resistance R for all voltage levels employed.
- Device stochastic switching behavior plus instrument induced noise are described by well behaved normal (Gaussian) distributions of the residual data points,

$$N_{sw}(v) = \Delta R_{exp}(v) - \Delta R_{mean}(v)$$

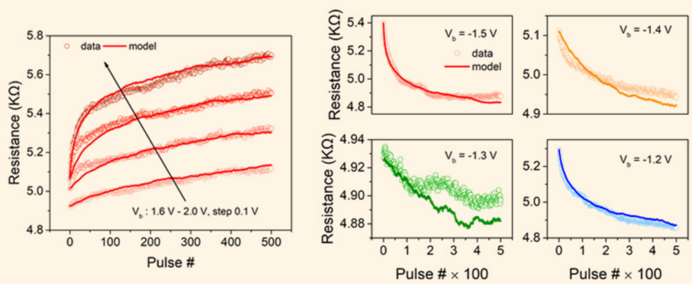
ΔR_{exp}: experimental amount of switching measurements

ΔR_{mean}: smoothed mean response (smoothed B-spline interpolation) of ΔR_{exp}.



Data Processing

- The standard deviation (SD) of the Gaussian fits showed a linear dependency on voltage.
- For each voltage polarity, the average value of the mean parameters of the distributions were considered.
- The extracted noise model was integrated in a recently presented Verilog-A ReRAM model [1] by using the built in function "**$rdist_normal(·)**".
- The model state variable is resistance so "**$rdist_normal(·)**" was simply added to the state variable derivative dR/dt.



Future Work and Conclusion:

The development of characterization algorithms and data analysis methods for isolating device stochasticity in resistive switching.
Investigation of the switching noise dependence on device resistive state.
Link of the extracted results with device physics.
Results verified the data-driven approach followed.
The simplicity of the method renders it fully compatible with modern ReRAM characterization systems.

References:

[1] I. Messaris et al. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. In press, 2018
[2] A. Serb et al. IEEE Transactions on Electron Devices. 62, 3685-3691, 2015
[3] Y. V. Pershin and M. Di Ventra. IEEE Transactions on Circuits and Systems I: Regular Papers. 57, 1857-1864, 2010
[4] R. Wizenberg et al. 2014 IEEE International Symposium on Circuits and Systems (ISCAS). 2269-2272, 2014