Dynamics of Memristor-based Memory Cells

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Introduction

Construction of memristive memories requires usage of stable and reliable individual memory devices. So far several technologies were tested to implement the memristive RRAM elements. Many of these use the metal-oxide/metal junctions. In this presentation we look into dynamic phenomena encountered in real memristors fabricated as solid state devices in the $Pt/HfO_2/Ti/Pt$ technology. The forming behaviour, the switching behaviour and repeatability of the process are tested. Further, we investigate phenomena associated with switching behaviour induced by voltage pulsing techniques. The pulsing technique allows for fast transition between the stable states characterised by different device resistances.

Research problems

- How stable are the resistive states in the bi-stable memristor?
- What are the characteristics when DC voltages are changed with a positive and negative ramp?
- Are multi-stable devices possible and what are the switching characteristics between the stable resistance states in multi-level memristive elements?
- What are the characteristics of the pulse programming operations?
- What is the width and amplitude dependence of the switching operations?
- What is the best characteristics for write-in and read-out?

Tested devices

- Each element implemented on the wafer consists of two crossing lines of Pt with a width ranging from 2 μm to 10 μm.
- The bottom 100 nm-thick lines of Pt were deposited by sputtering in a Pfeiffer SPIDER600 sputtering tool from a Pt target with 1000 W DC power.
- The bottom electrode is then patterned by optical lithography using AZ ECI 3007 resist and etched by chlorine plasma.
- Then, a 10 nm- thick HfO_2 layer is deposited by ALD with a BENEQ TFS200 from TEMAHf precursor and H2O reactant, followed by a 10 nm-thick Ti layer deposited by sputtering from a Ti target with 1000 W DC power.
- Subsequently, the top Pt electrodes are deposited with a similar recipe like for the bottom electrodes.
- Finally, both Pt and oxides are etched by chlorine plasma from STS dry etching tool, the end of oxide layer is detected by a built-in reflectometer

Conclusions

- The energy needed for switchings between stable states is relatively high
- Characteristics taken for the forcing by a voltage swing have been measured indicating that that when DC swings are applied the switchings appear at randomly changing voltage values.
- After a number of switchings the cells become worn-out

References

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Tested devices

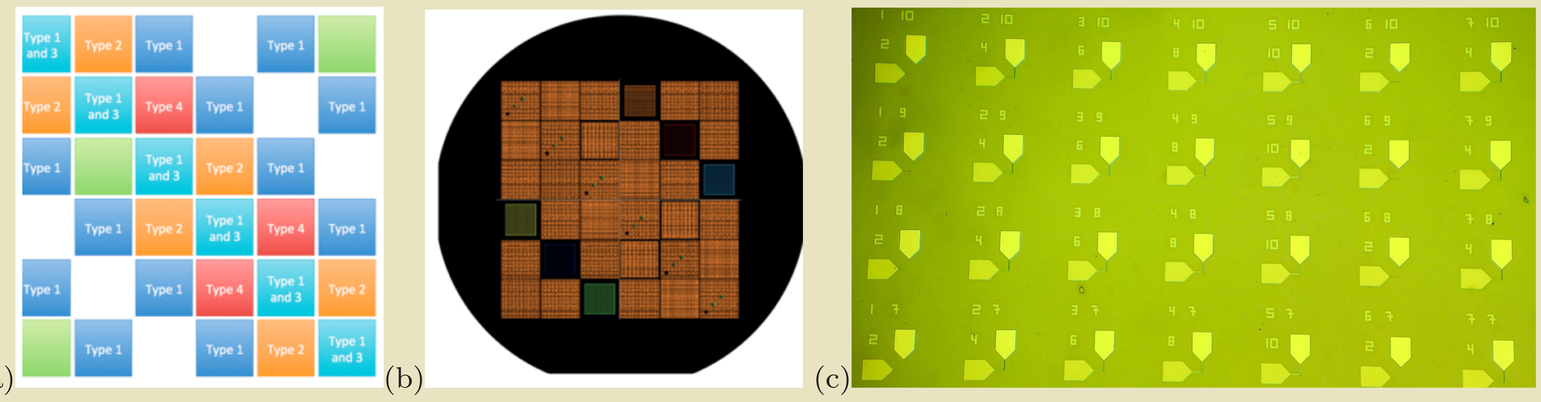

Figure 1: Layout of the wafer; a) Cadence view of the wafer, b) devices in each tiles, c) photograph of the elements (courtesy of Prof. Giovanni De Micheli from LSI EPFL)

Test results

All tests were carried out using the Keithley Model 4200-SCS Semiconductor Characterisation System and Arc One characterisation toolkit (courtesy Dr Themis Prodromakis from Nanofabrication Lab, Southampton University).

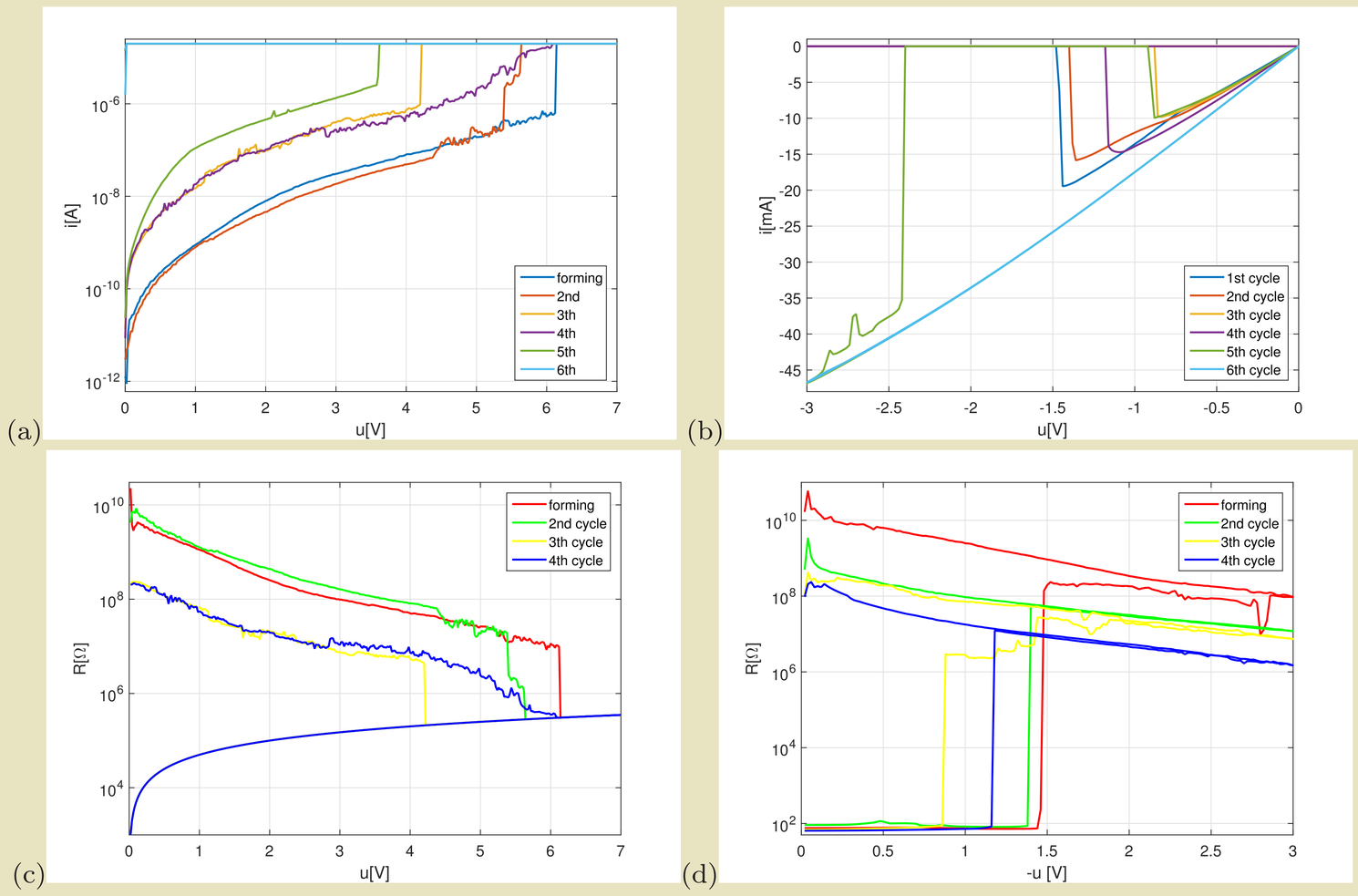

Figure 2: DC forcing - characteristics of switching process on the i-v plain (a,b). The device resistance changes during the switching process (c,d). Characteristics (a,c) presents the setting process of the device, while (b,d) resetting. Switchings appear at different non-repeatable voltage levels

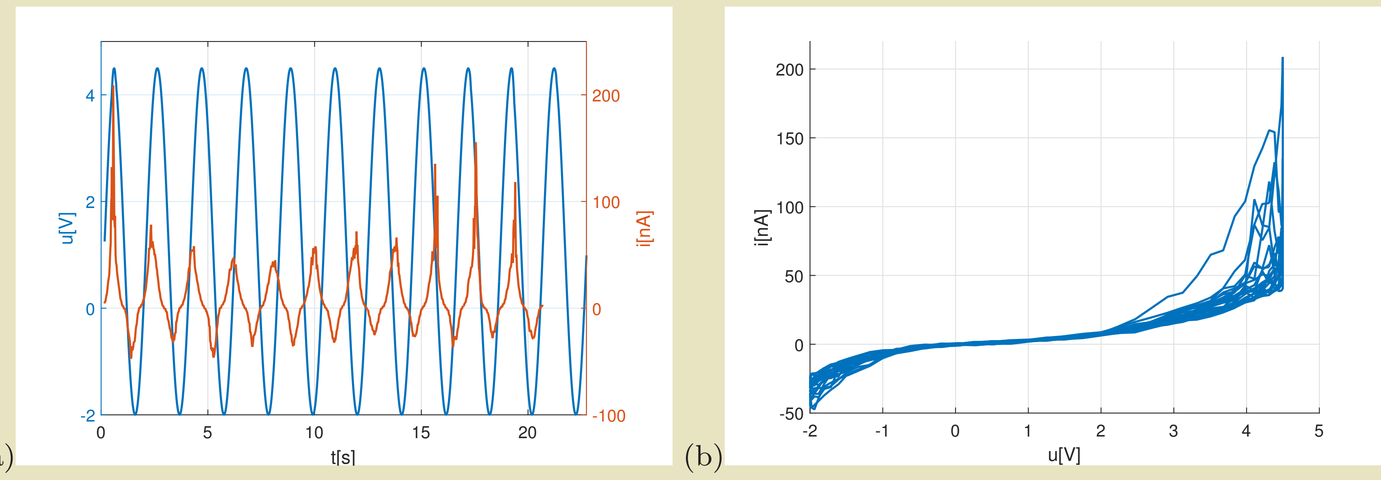

Figure 3: Sinusoidal responses. a) - time series of the applied voltage and responded current, b) i-v plot of the sinusoidal respond. When sinusoidal forcing is applied hysteretic behaviour becomes visible.

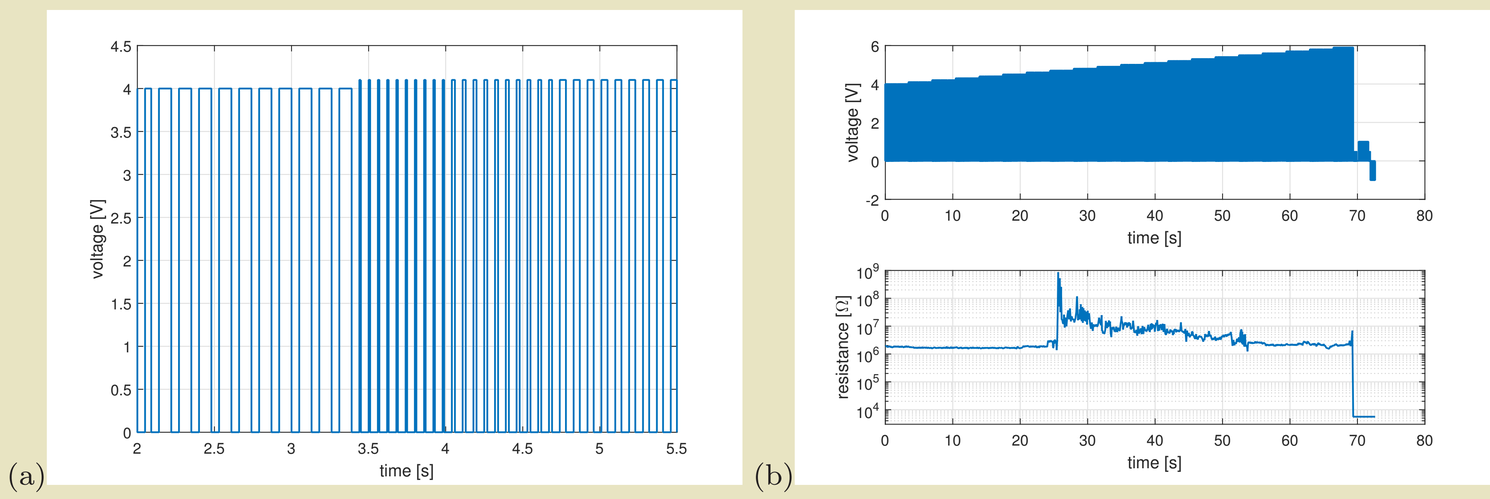

Figure 4: Programming the memory cell using pulses. a) the voltage pulses that were used to set the device. Both the pulses width and the amplitude were varied. b) the process of setting the device. Graph presents the applied voltage pulses series and the resistance of the tested device.